|  |  |
| --- | --- |
| Name: M Nabeel Zaib | EE-272L Digital Systems Design |
| Reg. No.: 2023-EE-067 | Marks Obtained: \_\_\_\_\_\_\_\_\_\_\_\_ |

**Lab Manual**

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| **DSD Lab Manual Evaluation Rubrics** | | | | | |
|  |  |  |  |  |  |
| **Assessment** | **Total Marks** | **Marks Obtained** | **0-30%** | **30-60%** | **70-100%** |
| Code Organization (CLO1) | 3 |  | No Proper Indentation and descriptive naming, no code organization.  Zero to Some understanding but not working | Proper Indentation or descriptive naming or code organization.  Mild to Complete understanding but not working | Proper Indentation and descriptive naming, code organization.  Complete understanding, and proper working |
| Simulation (CLO2) | 5 |  | Simulation not done or incorrect, without any understanding of waveforms | Working simulation with errors, don't cares's(x) and high impedance(z), partial understanding of waveforms | Working simulation without any errors, etc and complete understanding of waveforms |
| FPGA (CLO2) | 2 |  | Not implemented on FPGA and questions related to synthesis and implementation not answered. | Correctly Implemented on FPGA or questions related to synthesis and implementation answered. | Correctly Implemented on FPGA and questions related to synthesis and implementation answered. |

1. **Truth table of the circuit**

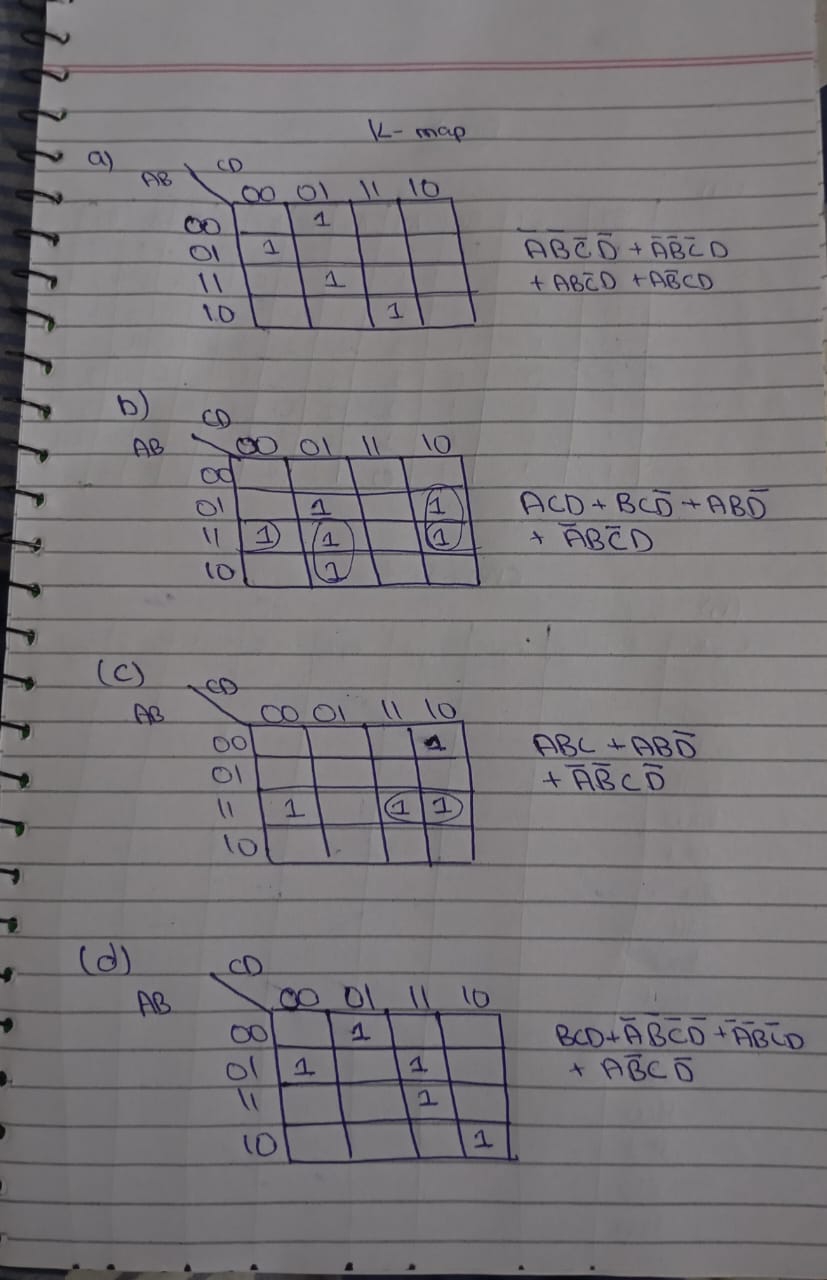
**ANODE**

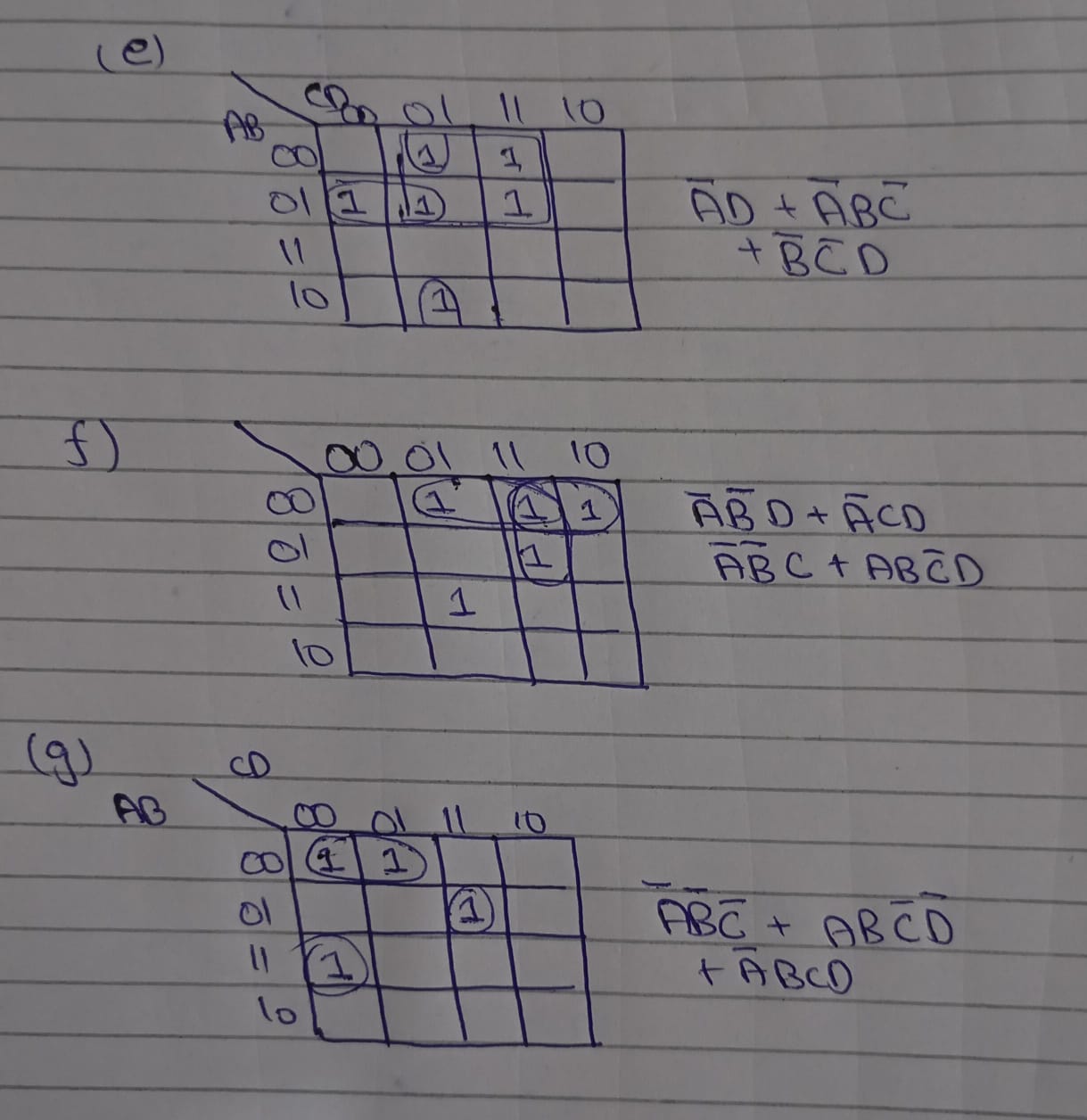
|  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| **S2** | **S1** | **S0** | **A7** | **A6** | **A5** | **A4** | **A3** | **A2** | **A1** | **A0** |
| **0** | **0** | **0** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **0** |
| **0** | **0** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **0** | **1** |
| **0** | **1** | **0** | **1** | **1** | **1** | **1** | **1** | **0** | **1** | **1** |
| **0** | **1** | **1** | **1** | **1** | **1** | **1** | **0** | **1** | **1** | **1** |
| **1** | **0** | **0** | **1** | **1** | **1** | **0** | **1** | **1** | **1** | **1** |
| **1** | **0** | **1** | **1** | **1** | **0** | **1** | **1** | **1** | **1** | **1** |
| **1** | **1** | **0** | **1** | **0** | **1** | **1** | **1** | **1** | **1** | **1** |
| **1** | **1** | **1** | **0** | **1** | **1** | **1** | **1** | **1** | **1** | **1** |

**CATHODE**

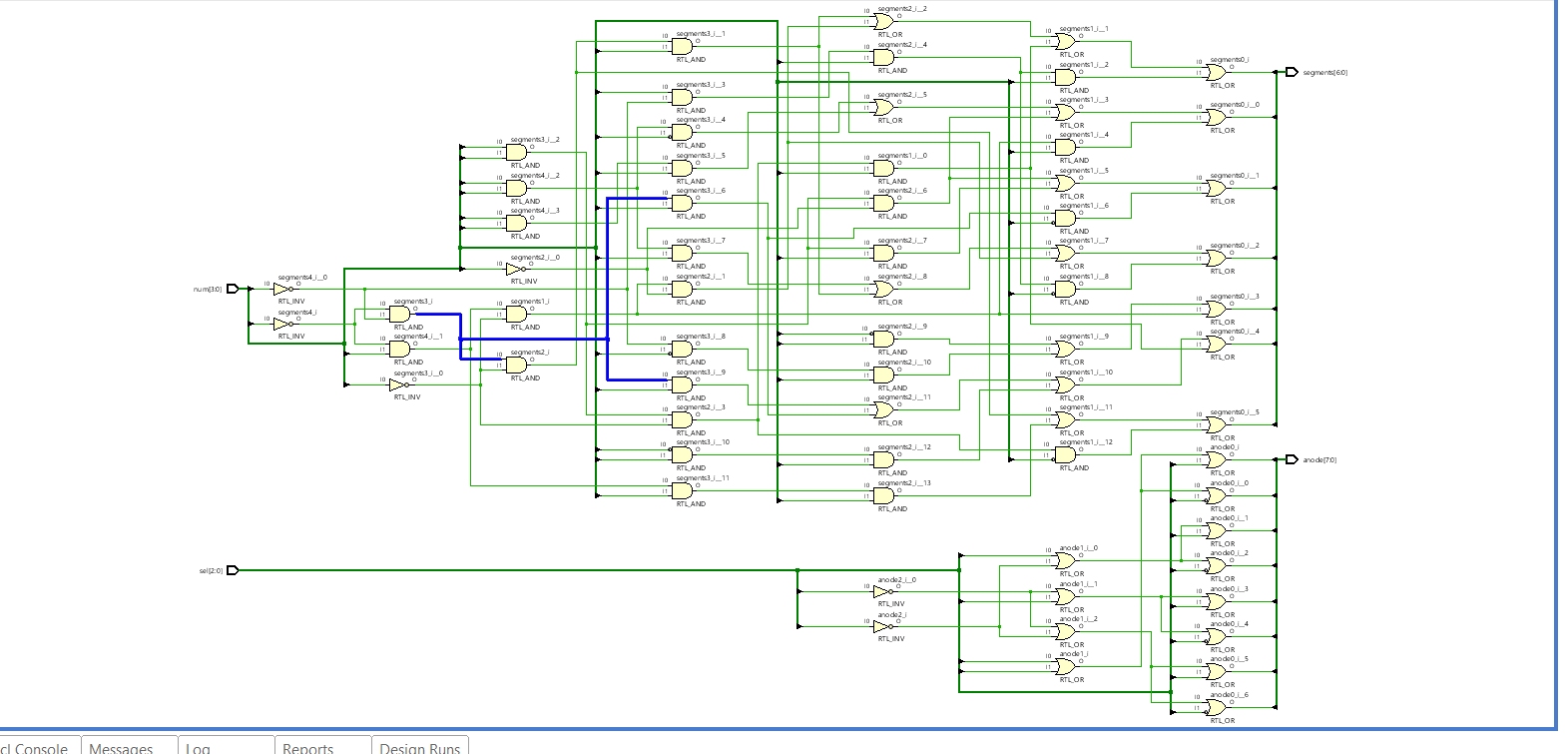
|  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- |
| **INPUT (4BITS)** | **HEX** | **Seg\_0** | **Seg\_1** | **Seg\_2** | **Seg\_3** | **Seg\_4** | **Seg\_5** | **Seg\_6** |
| **0000** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **1** |
| **0001** | **1** | **1** | **0** | **0** | **1** | **1** | **1** | **1** |
| **0010** | **2** | **0** | **0** | **1** | **0** | **0** | **1** | **0** |
| **0011** | **3** | **0** | **0** | **0** | **0** | **1** | **1** | **0** |
| **0100** | **4** | **1** | **0** | **0** | **1** | **1** | **0** | **0** |
| **0101** | **5** | **0** | **1** | **0** | **0** | **1** | **0** | **0** |
| **0110** | **6** | **0** | **1** | **0** | **0** | **0** | **0** | **0** |
| **0111** | **7** | **0** | **0** | **0** | **1** | **1** | **1** | **1** |
| **1000** | **8** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |
| **1001** | **9** | **0** | **0** | **0** | **0** | **1** | **0** | **0** |
| **1010** | **A** | **0** | **0** | **0** | **1** | **0** | **0** | **0** |
| **1011** | **B** | **1** | **1** | **0** | **0** | **0** | **0** | **0** |
| **1100** | **C** | **0** | **1** | **1** | **0** | **0** | **0** | **1** |
| **1101** | **D** | **1** | **0** | **0** | **0** | **0** | **1** | **0** |
| **1110** | **E** | **0** | **1** | **1** | **0** | **0** | **0** | **0** |
| **1111** | **F** | **0** | **1** | **1** | **1** | **0** | **0** | **0** |

**(PART B )K MAPS**

****

****

**SCHEMETIC**

****

**COMBINATIONAL DELAY**

**A screenshot of a computer

AI-generated content may be incorrect.**

**A screenshot of a computer screen

AI-generated content may be incorrect.**

**A table with numbers and letters

AI-generated content may be incorrect.**

THE maximum delay is from sell (2) to anode(6) is 11.094

**A screenshot of a computer

AI-generated content may be incorrect.**